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(54) **High density capacitive touch switch array arrangement**

(57) A capacitive touch switch arrangement is provided which alleviates panel layout problems which result from the minimum area required for proper operation of capacitive touch switches. There is at least a pair of capacitive touch switches, each having, as its input element, a touch pad (84 to 89) of sufficient area for proper operation of the touch switch. A pair of primary touch sensitive areas (58, 60, 62, 64, 66) are delineated, such as by panel indicia 69 to 77, and arranged such that a touch on either primary touch sensitive area activates only one of the respective touch switches. In addition, at least one secondary touch sensitive area (59, 61, 63, 65) is delineated and arranged such that a touch on the secondary touch sensitive area activates both of the adjacent touch switches. A circuit means responsive to the touch switches includes decoding logic for generating different outputs in response to the touching of each of the touch sensitive areas. Thus, there is not a one-for-one correspondence between all of the touch sensitive areas and the touch pads. In particular, there are more delineated touch sensitive areas than touch pads, and the touch sensitive areas may be smaller in area than the touch pads.

FIG. 3

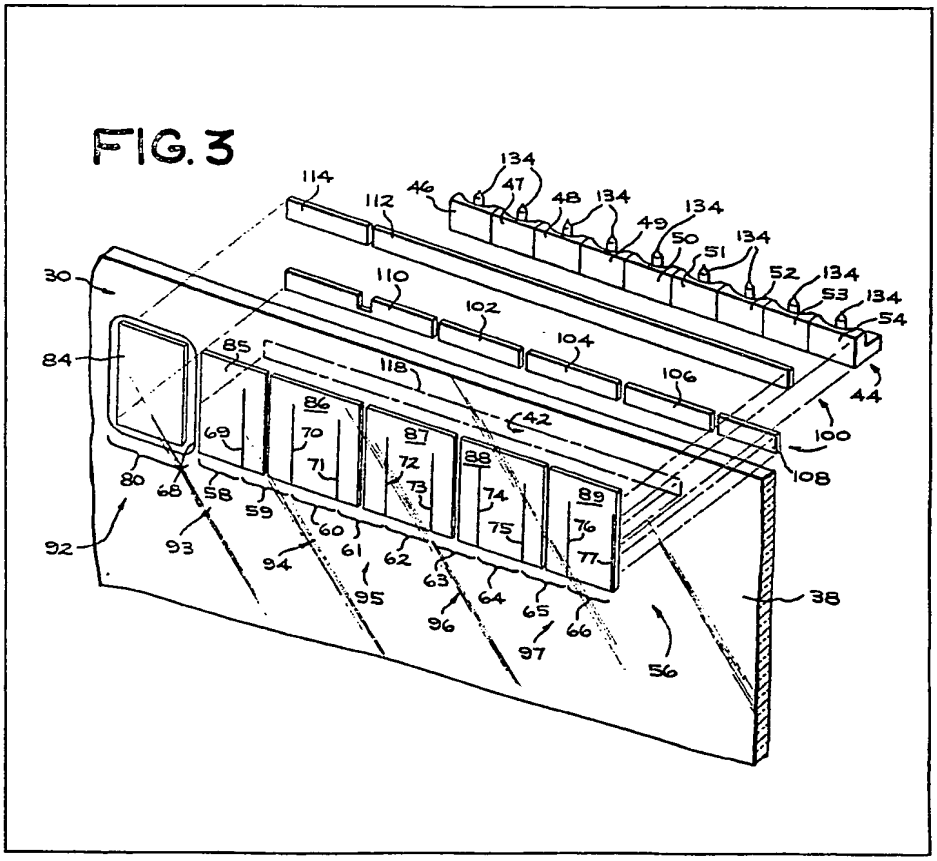

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FIG. 1

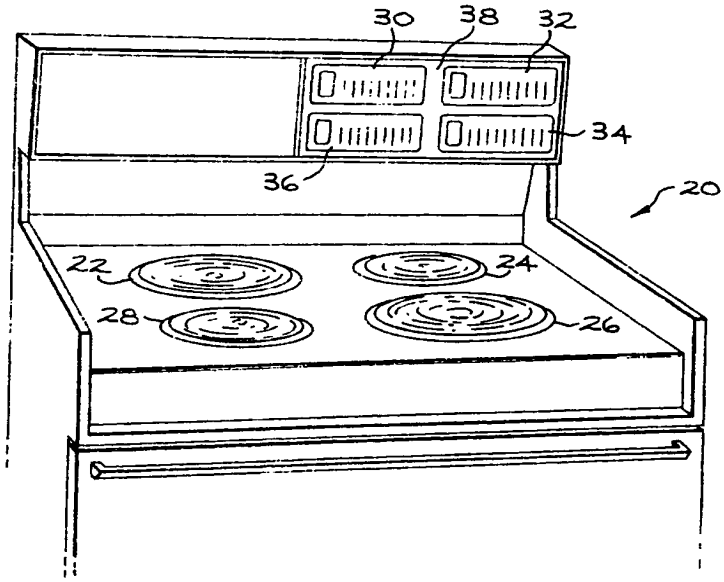


FIG. 2

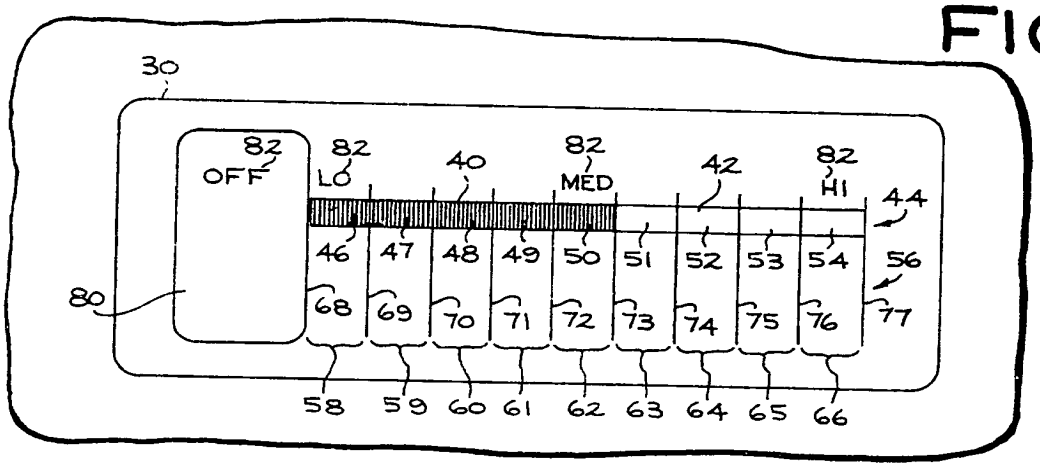


FIG. 11

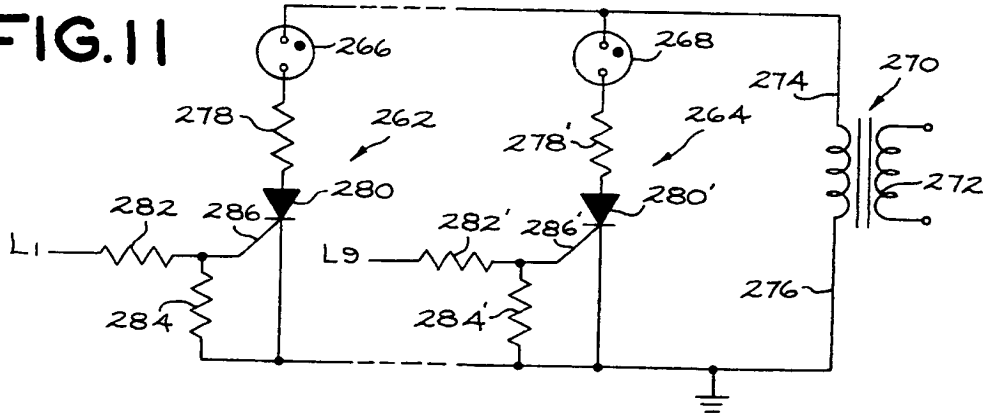


FIG. 3

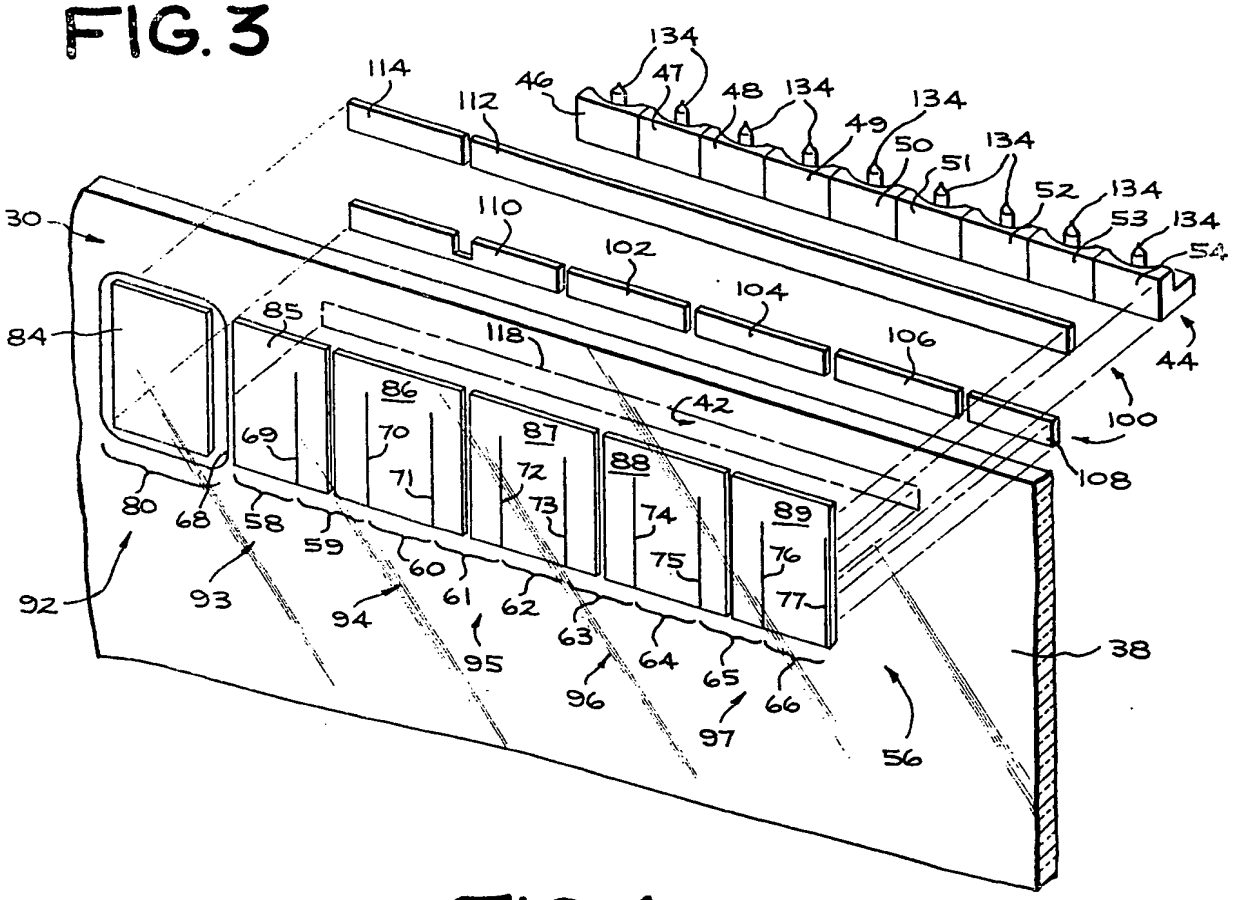
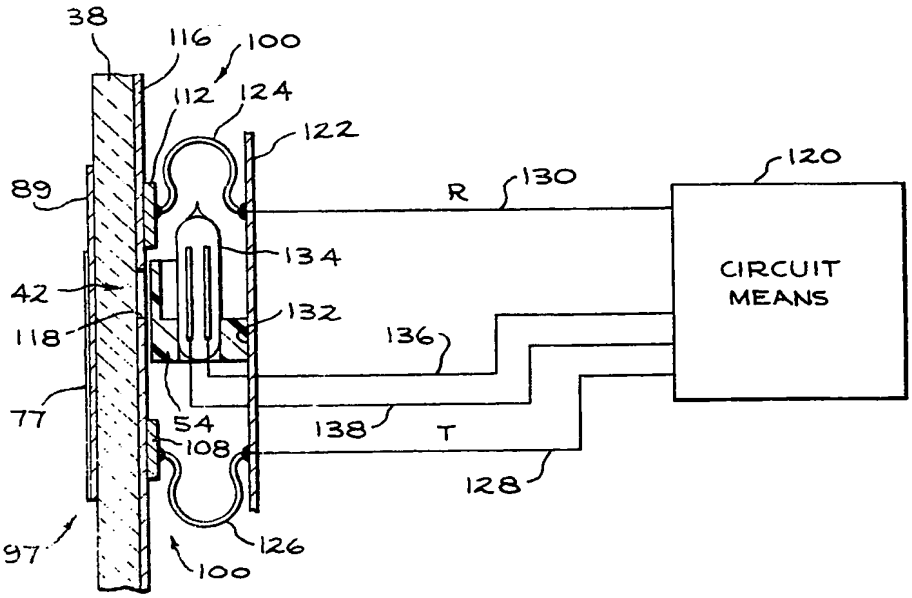


FIG. 4



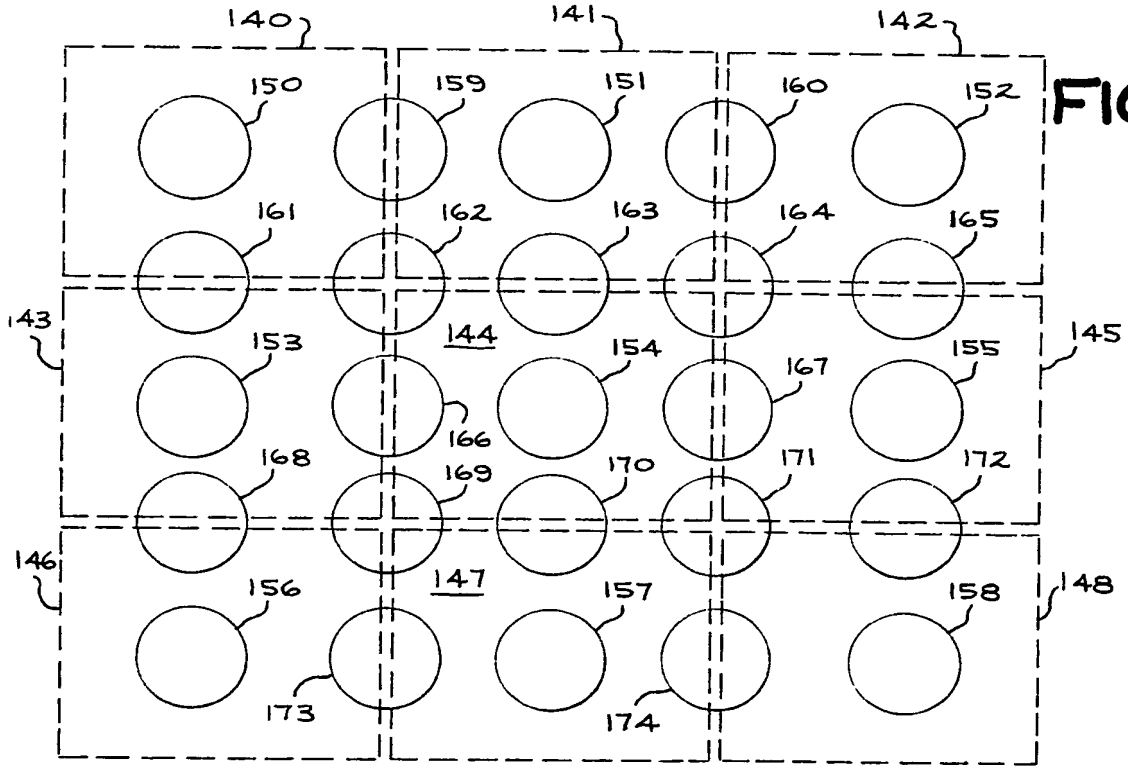


FIG.5

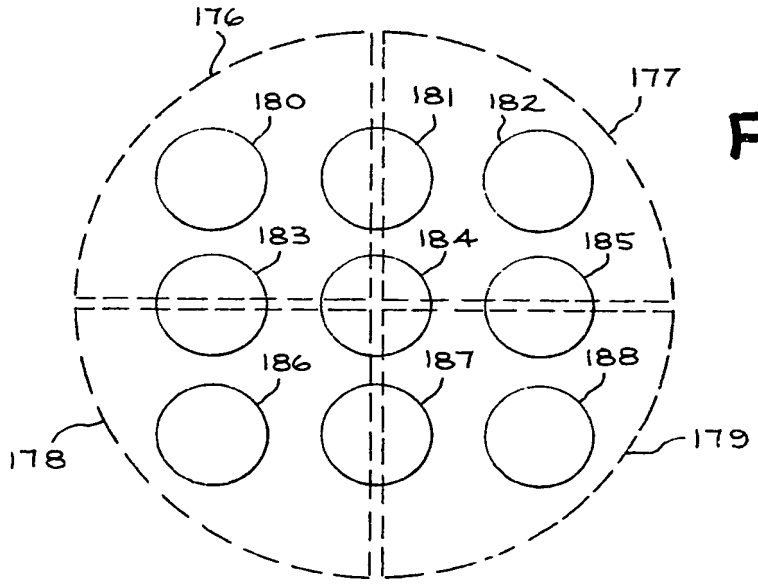


FIG.6

FIG.7

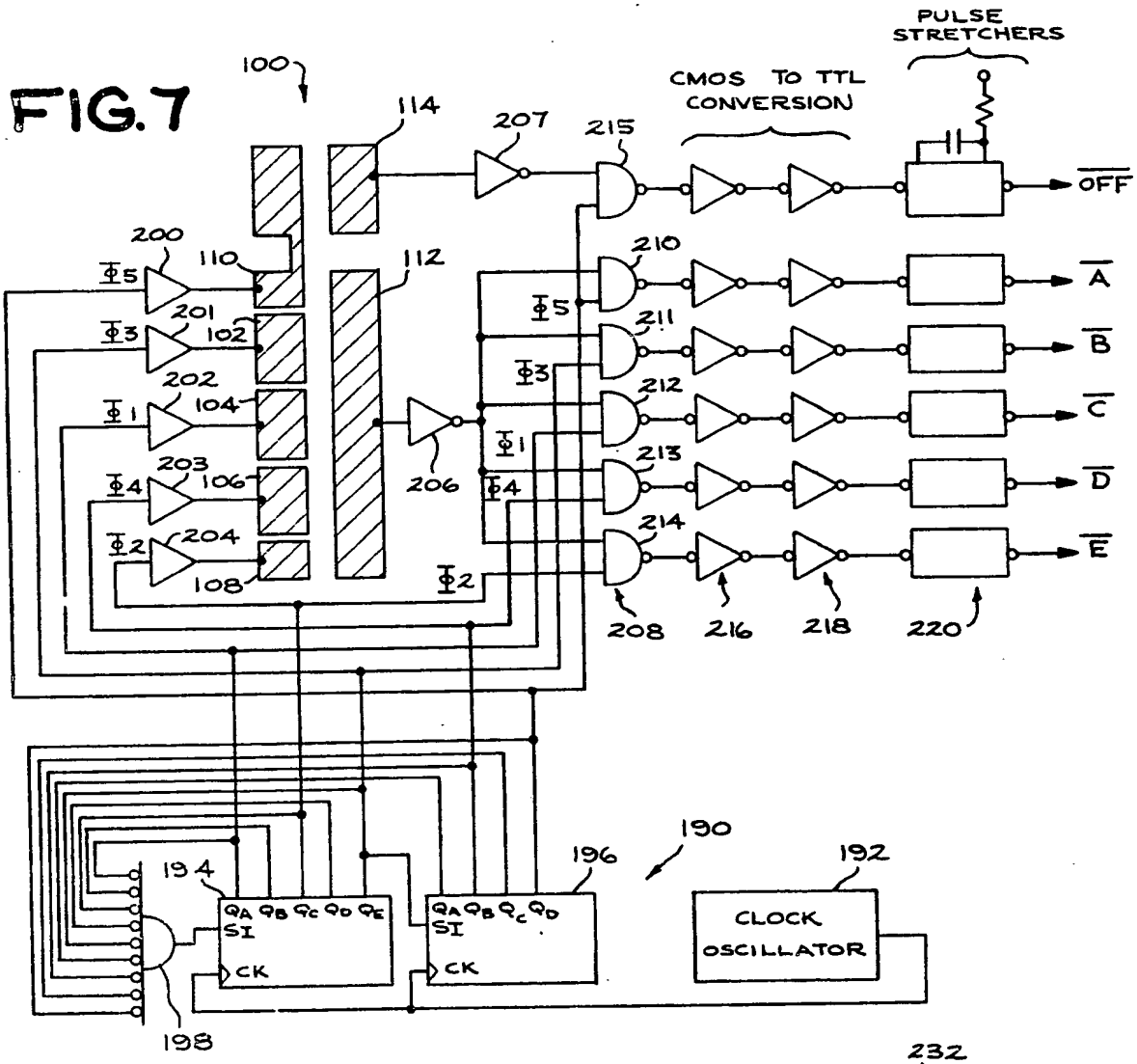


FIG.8

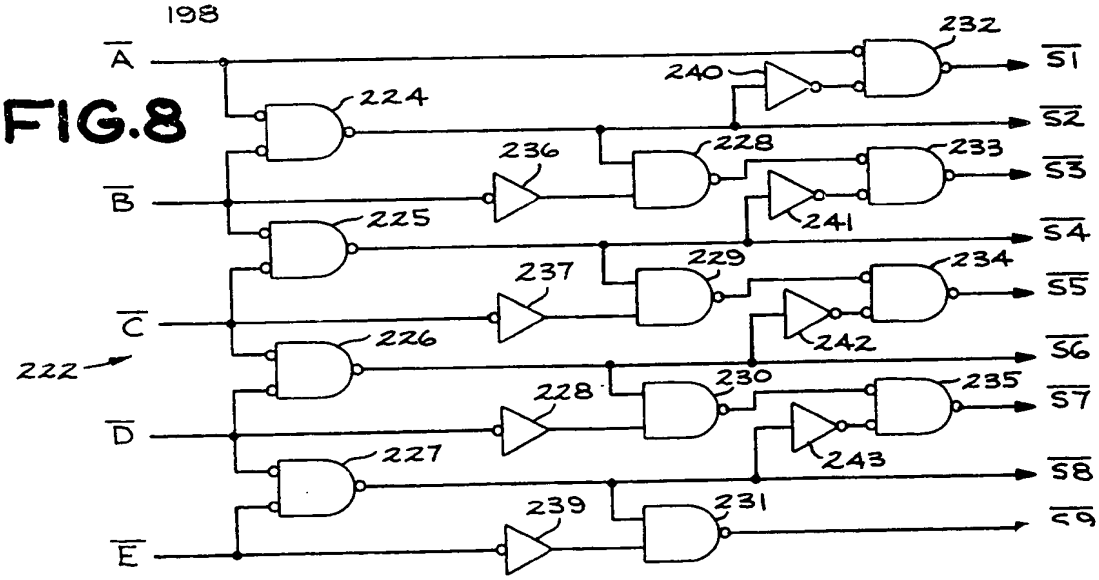


FIG. 9

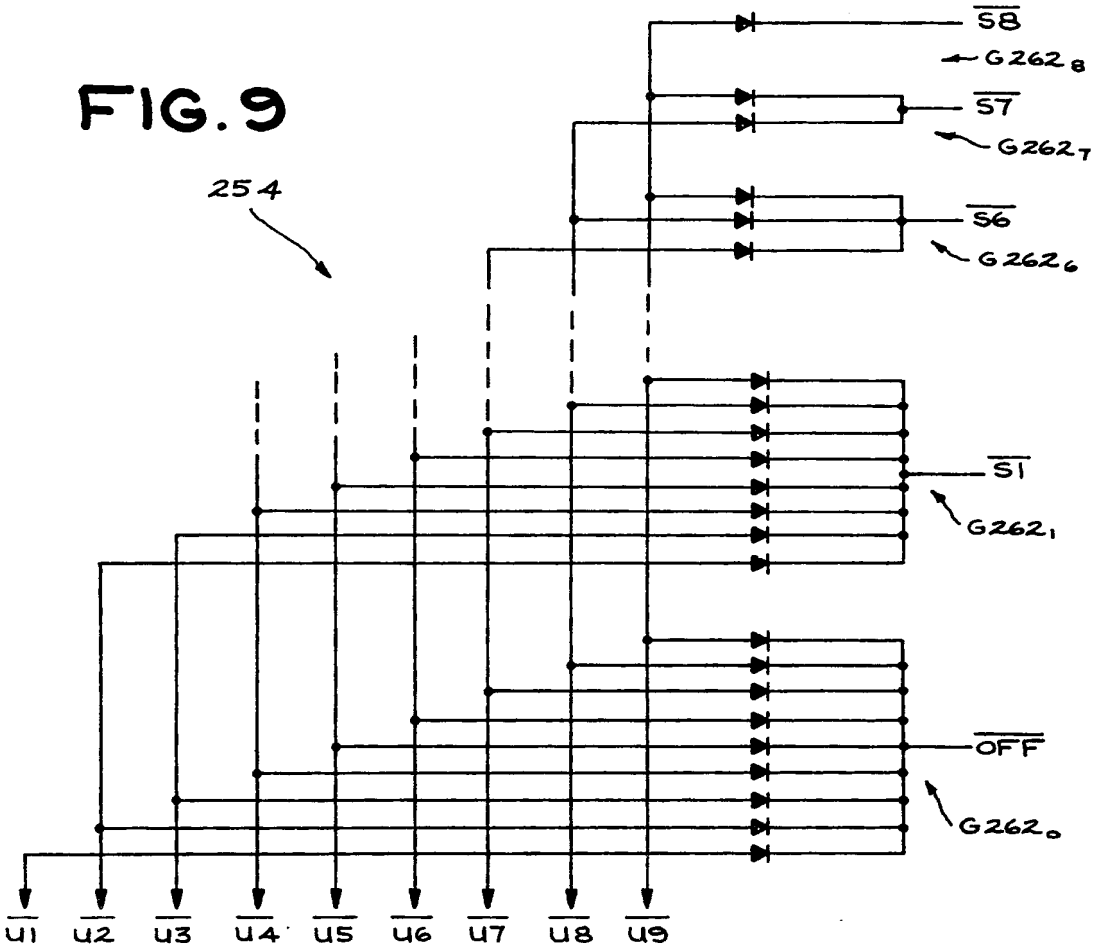
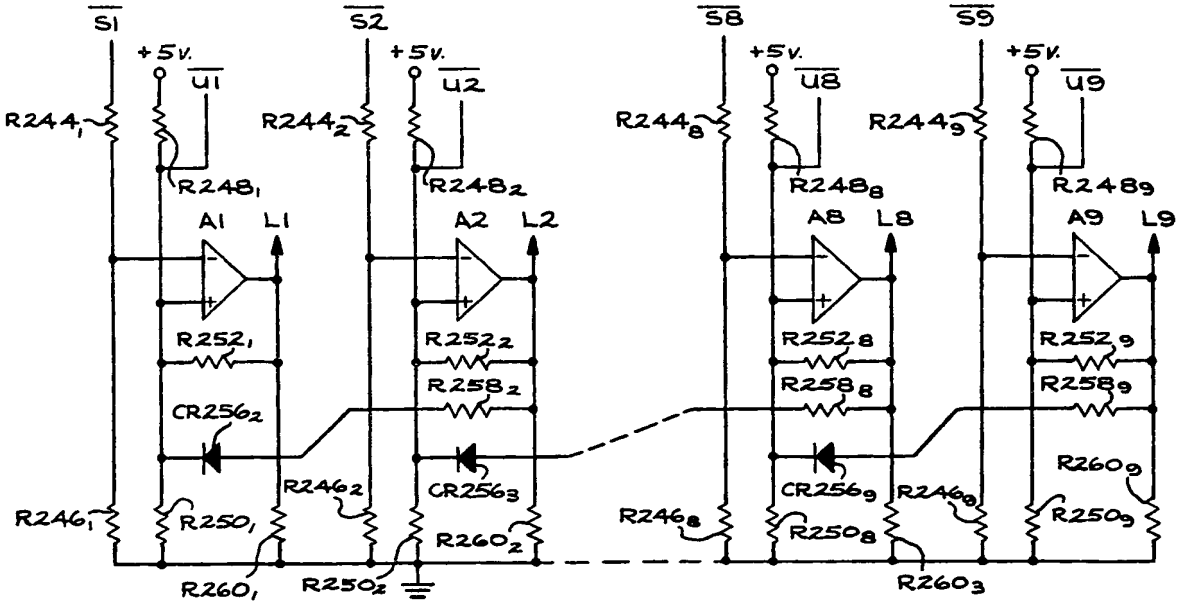


FIG. 10



SPECIFICATION

High density capacitive touch switch array arrangement

The present invention relates to capacitive data entry touch switches and, more particularly, to capacitive touch switch arrangements which alleviate limitations imposed by the minimum area required for proper operation of a capacitive touch switch.

Capacitive touch switches have recently come into use as user control inputs for appliances and the like. Their general advantages include making it possible to have a smooth control panel surface for good appearance and easy cleaning, eliminating reliability problems caused by mechanically movable switch contacts, and permitting convenient interface to circuitry in so-called "electronic" appliances.

Capacitive touch switch devices generally include a dielectric sheet element, for example a glass control panel. A conductive touch pad is disposed upon the front side of the panel. On the rear side of the panel just opposite the touch pad, there is disposed at least one conductive sensing pad. The front pad and the rear sensing pad thereby form the two plates of a capacitor, with the panel serving as the dielectric between the capacitor plates.

One specific type of capacitive touch switch is a "capacitive attenuator" switch which has two rear pads, one of which is a "transmitter" pad supplied with an AC signal at a frequency of approximately 20 KHz. The other rear pad is known as a "receiver" pad. In operation, so long as the front touch pad is not being touched, the AC signal is coupled through a capacitor formed by the transmitter pad and the front touch pad, and then through a capcitor formed by the front touch pad and the receiver pad, to appear on the receiver pad. When a person touches the touch pad, a portion of the AC signal is shunted to ground, causing the signal available at the receiver pad to decrease. This signal decrease is sensed by a signal loss detector, which then provides an output indicating the touch pad has been touched and the switch activated. While the particular embodiments described hereinafter employ capacitive attenuator type touch switches, there is another specific type of touch switch known as a "60 Hz pickup" to which the present invention is also applicable. In the "60 Hz pickup" type, stray AC fields are capacitively coupled by a person's touch to appear on the single rear pad. The resultant signal may be described as a "hum" and is familiar to anyone who has touched the input of a high gain audio amplifier. This hum-like signal is amplified and applied to the input of a signal threshold detector which, in response, produces a signal indicating that the touch pad has been touched.

With both of these touch switch types, the effectiveness and reliability of the switch depends upon sufficient signal being capacitively coupled through the panel dielectric to ensure reliable operation. For any given touch switch design there is a certain minimum value of capacitance required between the touch pad and each rear pad.

To achieve the minimum capacitances, a compromise must be made between two major design parameters: capacitor plate area and dielectric thickness. A formula for the capacitance of a two-plate capacitor is:

$$C = 0.224 \frac{KA}{d}, \text{ where}$$

C is the capacitance in picofarads (pf.);
K is the dielectric constant of the dielectric material between the plates;
A is the area of the smaller plate for example in square inches; and
d is the separation of the plates for example in inches

Thus, assuming the panel dielectric material remains the same, the capacitance value is directly proportional to plate area and inversely proportional to panel thickness. While, in the particular capacitive attenuator touch switch application, the exact value calculated from the above formula may be only approximate due to the partially overlapping nature of the front and rear pads, the proportional relationships with respect to capacitor plate area and panel dielectric thickness generally hold true.

For resistance to breakage, it is preferable that the panel be tempered glass in the order of at least 3/16 inch (4.7625 mm) thick. Thus as a practical matter in the design of a reliable system, it is the capacitor plate area parameter which must be selected. By way of specific example, in one particular system employing a 3/16 inch (4.7625 mm) thick tempered glass panel, the minimum area required for the touch pad was found to be 0.75 square inches (4.8387 cm^2) including the areas need to overlap both rear pads. For enhanced reliability, it is preferable that an even larger area be employed.

In the case of a capacitive attenuator type switch, it should be mentioned that the signal coupled through the switch can also be increased by simply increasing the AC exciting voltage applied to the transmitter pad. However, this approach is limited because, to avoid user discomfort from a slight electric shock, the AC exciting voltage applied to the transmitter pad should remain below approximately 200 volts.

This minimum area required for the touch pad heretofore has limited the use of capacitive touch switches when a large number of different entries are needed on a relatively small panel surface area. As one particular example, may have a linear array of nine adjacent touch switches superimposed over a lighted bar graph display. Each of the touch switch touch pads in that system defines a touch area corresponding to one of the segments of the bar graph. Since the touch switches are relatively narrow, to achieve the required

capacitor plate area for reliable operation the individual touch pads extend above and below the actual portions designated for touching. In particular applications, such an approach might be unsuitable because extensions of the touch pads encroach on panel area which might be desired for other purposes.

As another example, some control panels include a data entry portion comprising a three-by-three array for entering numerical digits "1" through "9". Again, the minimum area required for the capacitive touch pads has heretofore limited the use of capacitive touch switches to applications where sufficient panel area is available, for esthetic reasons or otherwise.

One embodiment of the invention comprises a capacitive touch switch arrangement including a pair of capacitive switches, each having, as its input element, a touch pad of sufficient area for proper operation of the touch switch. A pair of primary touch sensitive areas are delineated, such as by panel indicia, and arranged such that a touch on either primary touch sensitive area activates only one of the touch switches. In addition, a secondary touch sensitive area is delineated and arranged such that a touch on the secondary touch sensitive area activates both of the touch switches. A circuit means is responsive to the touch switches and includes decoding logic for generating different outputs in response to the touching of each of the touch sensitive areas. More specifically, the decoding logic is arranged such that when either touch pad is touched alone, an output signal representing the corresponding primary touch sensitive area is generated. When both of the touch pads are touched at the same time, an output signal representing the secondary touch sensitive area is generated.

The touch pads are located sufficiently close together so that they can be bridged by a single finger. Preferably, each of the primary touch sensitive areas is positioned over and is smaller than a corresponding one of the touch pads, and the secondary touch sensitive area is positioned at an interface between the touch pads so as to overlap both of the touch pads.

Instead of just two capacitive touch switches and three touch sensitive areas as described above, additional touch pads may be provided permitting various configurations of touch pad and touch sensitive area arrays. In every case, more touch sensitive areas than touch pads may be provided, with the result that the touch sensitive areas require less panel surface area than is requiredfor capacitive touch pad.

For example, and in accordance with another aspect of the invention, a linear touch switch array arrangement has a plurality of capacitive touch switches, each of which has, as the input element thereof, a touch pad of sufficient area for proper operation of the touch switch. The touch pads are arranged in the form of a linear array. Additionally, there is a linear array of delineated touch sensitive areas, including a plurality of primary touch sensitive areas corresponding in one-for-one relationship with the touch pads and arranged such that a touch on any one primary touch sensitive area activates only the corresponding touch switch, and additionally including a secondary touch sensitive area for each pair of touch pads and arranged such that a touch on the secondary touch sensitive area activates both of the touch switches for which the adjacent pair of touch pads are the input elements. Again, a suitable circuit is responsive to the touch switches and includes decoding logic for generating different outputs in response to touching of each of the touch sensitive areas. More specifically, the decoding logic is arranged such that when any single touch pad is touched an output signal representing the corresponding primary touch sensitive area is produced, and when any two adjacent touch pads are simultaneously touched an output signal representing the secondary touch sensitive area associated with the two touch pads is generated. Preferably, the primary touch sensitive areas are spaced from each, and the secondary touch sensitive areas are positioned in the spaces between the primary touch sensitive areas. Each of the primary touch sensitive areas is positioned over and narrower than its corresponding touch pad, and each of the secondary touch sensitive areas are overlappingly associated with both of the touch pads corresponding with the adjacent primary touch sensitive areas.

Briefly stated and in accordance with still another aspect of the invention, the bar graph type touch switch is improved by incorporating the linear touch switch array arrangement described immediately above as the touch input element thereof. In each of these embodiments it will be apparent that there is not a one-for-one correspondence between all of the touch sensitive areas and the touch pads comprising the input elements of the capacitive touch switches. In particular, there are more touch sensitive areas than touch pads, and the touch sensitive areas are smaller in the area than the touch pads.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings in which:-

Figure 1 is a perspective view of a portion of an electric range including bar graph type touch switch and display devices as the four surface unit heat controls, the devices incorporating the present invention;

Figure 2 is a greatly enlarged view of a single one of the touch switch and display devices of Figure 1 as it appears to the user when a "medium" heat setting has been selected;

Figure 3 is an exploded perspective view of the device of Figure 2, showing details of construction not ordinarily visible to the user;

Figure 4 is a sectional side view viewed from the right hand side of Figure 3, and further showing a subpanel and a block schematic representation of circuit means forming part of a complete operative device;

Figure 5 is a front panel view of another embodiment of the invention which has twenty-five individual touch sensitive areas arranged in a five-by-five array, but which requires only nine individual touch pads, arranged in a three-by-three array;

Figure 6 is a front panel view of an embodiment similar to that of Figure 5, except that only nine touch sensitive areas are provided, requiring only four touch pads;

Figure 7 is a portion of schematic diagram of a representative electrical circuit suitable for operating the embodiment of Figures 3 and 4;

Figure 8 is a further portion of the schematic diagram and, more specifically, the decoding logic portion thereof; and

Figures 9, 10 and *11* show circuitry suitable for receiving the outputs of the logic circuit of Figure 8 and for driving the indicator lamps of Figures 3 and 4 to and from a bar graph display.

Referring first to Figure 1, an electric range 20 includes four conventional electric surface heating units 22, 24, 26 and 28. To provide user control over the heat produced by the surface heating units. Four corresponding input/output devices 30, 32, 34 and 36 are disposed upon the right hand portion of the range control panel 38, which is formed of tempered glass approximately 3/16 inch (4.7625 mm) thick for good appearance and cleanability. As will be apparent from the physical arrangement of the devices 30, 32, 34 and 36, the upper left input/output device 30 controls the left rear surface heating unit 22, the upper right input/output device 32 controls the right rear surface heating unit 24, and so on.

Referring now to Figure 2, there is shown a greatly enlarged view of representative input/output device 30 as it appears to the user when a "medium" heat setting for the left rear surface heating unit 22 has been selected. To indicate to the user what heat setting has been selected, a lighted bar graph display 40 is visible through a suitable transparent window 42 in the panel 38. The illustrated bar graph display 40 employs a red light bar, as symbolized by the vertical line shading. The bar graph display 40 actually comprises a linear array 44 of individual display segments 46 through 54 which are strung out such that each segment is adjacent to no more than two other segments. The segments are adapted to be progressively energized to form the bar graph type display 40 representing a numerical quantity.

In order to provide user input to the device 30, a linear array 56 of light transmitting touch sensitive areas 58 through 66 is superimposed over the array 44 of display segments. The individual touch sensitive areas 58 through 66 are delineated by lines 68 through 77 forming the left and right boundaries of the invdividual touch sensitive areas 58 through 66. It will be apparent however that many different means of delineating the individual touch sensitive areas 58 through 66 are possible. One other example is a dot or line marking the center of each of the touch sensitive areas, with the exact boundary not being precisely identified. Such a center mark would still direct a person's finger to the appropriate touch sensitive area. The delineating lines 68 through 77 may be applied in any suitable manner such as painting or silk screening.

To provide a means for turning the surface heating unit 22 completely off, an "OFF" touch sensitive area 80 is positioned at the extreme left hand side of the display segment array 44 and the touch area array 56, the "OFF" touch sensitive area being delineated by an extension of the line 68 to form a rectangle. Since no corresponding display segment is associated with the "OFF" touch sensitive area 80, it may or may not be transparent. Finally, a legend 82 in the form of "OFF," "LO," "MED" and "HI" symbols is applied to the control panel 38.

Turning now to Figures 3 and 4, the underlying constructional details of the representative input/output device 30 may be seen. Figure 3 is an exploded perspective view of the various elements associated most directly with the glass panel 38, and Figure 4 is a sectional right side view of the panel as assembled, together with additional elements.

Disposed on the front side of the panel 38 are six touch pads 84 through 89 which comprise the input elements of capacitive touch switches generally designated 92 through 97. It will be apparent that the thicknesses of the touch pads 84 through 89 are greatly exaggerated for clarity of illustration. Considering particularly the touch pads 85 through 89, these pads are arranged in the form of a linear array and each is of sufficient area for proper operation of the touch switch of which it comprises the input element. The touch pads 85 through 89 may be formed of an electrically conductive material which an be metalized or deposited on the front surface of the panel 38 in a sufficiently thin layer so as to be substantially transparent. One example of a suitable conductive material is tin oxide.

To complete the touch switches 92 through 97, conductive rear pads, generally designated 100, are disposed on the rear side of the panel 38. More specifically, individual transmitter pads 102, 104, 106 and 108 are provided for the touch switches 94, 95, 96 and 97, respectively. A single split transmitter pad 110 serves both the touch switches 92 and 93. A single receiver pad 112 serves the five touch switches 93 through 97 through a multiplexing arrangement hereinafter described. The "OFF" touch switch 92 has an individual receiver pad 114. It will be seen that each of the rear pads 100 thereby forms a capacitor with at least one of the touch pads disposed on the front side of the panel 38.

In the particular arrangement illustrated, the rear pads 100 need not be transparent and therefore may be made of any suitable conductive material, such as metallic silver or copper. In order to conceal the rear pads 100 from view for a pleasing appearance, a layer 116 of black paint (Figure 4) is applied to the rear side of the panel 38, underneath the rear pads 100, the window 42 being defined by a suitable break 118 in the paint layer 116.

The nature of the conductive touch pads 84 through 89 is such that they are not readily visible to the casual observer, but are discernible only upon close examination. However, the painted lines 68 through 77 delineating the individual touch sensitive areas 58 through 66 and the "OFF" touch sensitive area 80 are readily visible and, in conjunction with the visible outline of the window 42, guide a person's touch.

To facilitate electrical connection between the rear pads 100 and a circuit means 120, an electrically insulating subpanel 122 (Figure 4) is mounted behind and spaced from the rear panel 38. The subpanel 122

carries suitable spring contact clips such as the clips 124 and 126 which contact the rear pads 100. Representative transmitter (T) and receiver (R) conductors 128 and 130 connect the spring contact clips 126 and 124 to the circuit means 120.

The subpanel 122 additionally carries the individual display segments 46 through 54 comprising the array 44. In Figure 4, the representative display segment 54 is joined to the subpanel 122 at 132 by any suitable means such as by gluing. In Figures 3 and 4, each of the individual display segments 46 through 54 may be seen to comprise a neon lamp 134 mounted in a suitable red plastic light dispersing lens element. The lens elements are preferably rectangular when viewed from the front thereof, and have suitable light scattering surface roughness so as to produce a solid block of light when the neon bulbs 134 are energized. To complete the mechanical arrangement, conductors 136 and 138 connect the electrodes of the representative neon lamp 134 in Figure 4 to the circuit means 120.

In the operation of the touch switch and display device 30 and more particularly of the array 56 of light transmitting touch sensitive areas 58 through 66 and the associated touch pads 85 through 89, when a user touches any one of the individual touch sensitive areas 58 through 66, the circuit means 120 responds to properly drive the display array 44 to form a bar graph. Additionally, the circuit means 120 sends suitable signals to external circuitry (not shown) to cause the appropriate control function, for example establishing a desired heat setting, to be accomplished.

In accordance with the present invention, fewer touch pads 85 through 89 than delineated touch sensitive areas 58 through 66 are required. More particularly, the array 56 of touch sensitive areas includes a plurality of primary touch sensitive areas 58, 60, 62, 64 and 66 arranged such that a touch on any one primary touch sensitive area activates only the corresponding touch switch. The primary touch sensitive areas 58, 60, 62, 64 and 66 are spaced from each other and each is positioned over and narrower than its corresponding touch pad. It can be seen that the primary touch sensitive area 58 corresponds with the touch pad 85, the primary touch sensitive area 60 corresponds with the touch pad 86, the primary touch sensitive area 62 corresponds with the touch pad 87, the primary touch sensitive area 64 corresponds with the touch pad 88, and the primary touch sensitive area 66 corresponds with the touch pad 89.

The array 56 of touch sensitive areas further includes secondary touch sensitive areas 59, 61, 63 and 65, each of the secondary touch sensitive areas being for an adjacent pair of touch pads and arranged such that a touch on the secondary touch pad activates both of the touch switches for which the adjacent touch pads are the input elements. More particularly, the secondary touch sensitive areas 59, 61, 63 and 65 are positioned in the spaces between the primary touch sensitive areas 58, 60, 62, 64 and 66 and overlappingly associated with both of the touch pads corresponding with the adjacent primary touch sensitive areas. For example, the secondary touch sensitive area 59 is positioned in the space between the primary touch sensitive areas 58 and 60 and overlappingly associated with the two touch pads 85 and 86 which correspond with the adjacent primary touch sensitive areas 58 and 60. It can be seen that a finger touching the secondary touch sensitive area 59 bridges both touch pads 85 and 86 to activate both of the touch switches 93 and 94.

The remaining secondary touch sensitive areas 61, 63 and 65 are similarly arranged. A touch on the secondary touch sensitive area 61, which is overlappingly associated with the touch pads 86 and 87, activates both touch switches 94 and 95. A touch on a secondary touch sensitive area 63 activates the touch switches 95 and 96. Lastly, a touch on the secondary touch sensitive area 65 activates the two touch switches 96 and 97.

Decoding logic (described later with particular reference to Figure 8) within the circuit means 120 is arranged such that when any single one of the touch pads 85 through 89 is touched, an output signal representing the corresponding primary touch sensitive area 58, 60, 62, 64 or 66 is produced. When any two adjacent touch pads are simultaneously touched, an output signal representing the secondary touch sensitive area 59, 61, 63 or 65 associated with the two touch pads is generated. The different signals thus generated by the decoding logic are applied to a means (described hereinafter with particular reference to Figures 9-11) for energizing the display segments 46 through 54 to produce the bar graph display.

As one particular example, if the primary touch sensitive area 62 is touched, only the touch switch 95 is activated and the logic means responds to produce a signal representing the primary touch sensitive area 62. The signal in turn is used to energize the display segment 50 and all display segments to the left, to produce the result depicted in Figure 2. If however the secondary touch sensitive area 63 is touched, then both the touch switches 95 and 96 are activated, and the control logic responds by generating a signal representing the secondary touch sensitive area 63. The display segment 51 is then additionally energized.

Referring now to Figure 5, there is shown a representation of an embodiment of the invention which permits twenty-five individual touch sensitive areas to be decoded while employing only nine actual touch pads. More specifically, there are provided nine touch pads 140 through 148, each of which is the input element of a capacitive touch switch. As before, the touch pads 140 through 148 are discernible only upon close examination. A plurality of delineated primary touch sensitive areas 150 through 158 are arranged in one-for-one correspondence with the touch pads 140 through 148 such that a touch on any one of the primary touch sensitive areas 150 through 158 activates only the touch switch associated with the corresponding one of the touch pads 140 through 148. In addition, a plurality of delineated secondary touch sensitive areas 159 through 174 are arranged such that a touch on any one of said secondary touch sensitive areas 159 through 174 activates at least two touch switches. From Figure 5, it can be seen that for each individual one of the touch sensitive areas 150 through 174, a unique combination of touch pads 140 through

148 is touched, resulting in a unique combination of activation of the underlying touch switches. With suitable decoding logic these individual combinations may be recognized to produce corresponding outputs.

The input expansion afforded by the present invention is quite apparent from a large array such as is depicted in Figure 5. It will be apparent that many more individual inputs can be combined on a single control panel of limited area where the present invention is employed than would be possible if individual touch switches not employing decoding according to the present invention were provided. For a regular two-dimensional array such as is illustrated in Figure 5, the precise expansion possible may be calculated using the following equation:

Total number of touch sensitive areas = $(2m - 1)(2n - 1)$,
Where m and n are the dimensions of the underlying array of touch pads.

Figure 6 is another example, which may be recognized as a simplification of the Figure 5 embodiment. From Figure 6 it may be seen that with four touch pads 176 through 179, nine individual touch sensitive areas 180 through 188 may be defined. In accordance with the nomenclature employed above, the touch sensitive areas 180, 182, 186 and 188 may be considered primary touch sensitive areas corresponding on a one-for-one basis with the touch pads 176, 177, 178 and 179. The remaining touch sensitive areas 181, 183, 184, 185 and 187 are then the secondary touch sensitive areas.

Referring now to Figures 7-11, one example of suitable circuitry for operating the input/output device 30 of Figures 2-4 will be described. It will be appreciated that the circuitry illustrated and described is exemplary only and that many different schemes are possible, including microprocessor based systems executing a sequence of instructions stored in a program memory.

In Figure 7, the rear transmitter pads 110, 102, 104, 106 and 108 of Figure 3 are represented, along with suitable circuitry for driving the transmitter pads. Similarly, the rear receiver pads 112 and 114 are represented along with suitable circuitry connected to receive the outputs therefrom. The touch pads 84-89 visible in Figure 3 are not shown in Figure 7.

The embodiment described herein uses a multiplexing technique which requires significantly fewer electrical connections between the circuitry itself and the rear pads 100. However, as previously stated, the specific circuitry described herein is exemplary only and specific circuit details, including the multiplexing arrangement, are not a part of the invention claimed herein.

The digital logic elements employed nerein are of two families: CMOS and TTL. The CMOS logic may comprise elements selected from the CD-4000 series of integrated circuits manufactured by RCA Corporation, and the TTL logic elements may comprise SN7400 series integrated circuits manufactured by Texas Instruments, Inc.

Considering specifically the transmitter circuitry of Figure 7, a five-phase clock, generally designated 190, comprises a suitable square wave oscillator 192 operating on a frequency of approximately 100 KHz, and a pair of serially connected five-bit shift registers 194, 196 with their clock (CK) inputs driven by the clock oscillator 192. The five-bit shift registers 194 and 196 may comprise SN7496 TTL IC's. To prevent overlapping outputs, every other shift register output along the chain is taken to provide the five clock phase outputs. Specifically, from the first five-bit shift register 194, the Q_A output drives the $\Phi 1$ line, the Q_C output drives the $\Phi 2$ line, and the Q_E output drives the $\Phi 3$ line. From the second five-bit register 196, the Q_B line drives the $\Phi 4$ line and the Q_D output drives the $\Phi 5$ line. The Serial Input (SI) of the first shift register 194 receives the output of a nine input, low-activated AND gate 198 having its inputs connected to the Q_A through Q_E outputs of the first shift register 194 and the Q_A through Q_D outputs of the second shift register 196.

The logical equivalent of the low-activated AND gate 198 may be constructed from three SN7427 TTL 3-input NOR gates supplying the inputs of an SN7410 TTL 3-input NAND gate followed by an SN7404 TTL inverter.

In the operation of the five-phase clock 190, logic highs are applied to the serial input (SI) of the first shift register 194 and is clocked through in response to pulses from the clock oscillator 192 to successively appear at each of the Q outputs. Upon initial powering up of the circuit, the output of the AND gate 198 remains low, and this low applied to the first shift register 194 SI input causes all the shift register stages to eventually be cleared to logic low in response to clock pulses. When all the Q outputs are low, the output of the low-activated AND gate 198 goes high, inserting a logic high into the A stage of the first shift register 194, and this logic high is then clocked through in response to clock pulses.

The five clock lines are applied to the inputs of five transmitter pad drivers 200 through 204, which have their outputs connected to the transmitter pads 110, 102, 104, 106 and 108. The drivers 200 through 204 have high voltage transistor outputs, and provide approximately 160 volts to the transmitter pad.

The common receiver pad 112 is connected to a high impedance input inverter/buffer amplifier 206, and the "OFF" receiver pad 114 to another high impedance input inverter/buffer amplifier 207. Both inverters 206 and 207 may comprise CD4049 CMOS IC's. A de-multiplexing network 208 comprises five NAND gates 210 through 214, each of which has its upper input connected to the output of the common buffer amplifier 206 and its lower input connected to one of the clock phase lines $\Phi 1$ through $\Phi 5$. For the "OFF" touch switch, another NAND gate 215 has its upper input connected to the output of the inverter 207, and its lower input to the clock phase line $\Phi 5$. The NAND gates 210 through 215 may comprise CD4011 CMOS NAND gates.

In the operation of the de-multiplexing network 208, each of the NAND gates is interrogated in sequence by a logic high on the corresponding one of the clock lines Φ1 through Φ5. If the corresponding touch pad is not touched, the logic high present on the corresponding transmitter pad is capacitively coupled to the common receiver pad 112, changed to logic low by the inverter 206, and applied to the upper input of the corresponding one of the NAND gates 210 through 214. The NAND gate is not activated and its output therefore remains high. If, however, one or more of the touch pads is touched, then the logic high applied to the receiver pad in response to the particular clock phase is shunted by the touch. The receiver pad 112 goes low. The resultant logic high at the output of the inverter 206 applied to the upper input of the corresponding NAND gate of the de-multiplexing network 208 in coincidence with a logic high from the particular clock phase line causes the output of the NAND gate of the de-multiplexing network 208 to go low, indicating that the corresponding touch switch has been activated. The NAND gate 215 for the "OFF" touch switch operates similarly.

The outputs of the NAND gates 210 through 215 are applied through first and second sets of buffers 216 and 218 to effect CMOS to TTL conversion. The first buffers 216 may be the type CD4050 CMOS buffers, and the second buffers 218 may be type SN7407 TTL buffer amplifiers. Suitable output pull up resistors are required.

To enhance noise immunity, the outputs of the buffers 218 are followed by a set of pulse stretchers 220. Each of the pulse stretchers 220 may comprise for example a type SN74123 TTL re-triggerable monostable multivibrator, with suitable external resistance and compacitance to provide an output pulse of 30 microseconds duration when triggered. To provide low active inputs and low active outputs of the pulse stretchers 220, the "A" inputs of the SN74123 IC's are used, and the $\overline{Q}$ outputs are used.

The output lines of the pulse stretchers 220 are designated $\overline{OFF}$ and $\overline{A}$ through $\overline{E}$. Each of these lines goes low when the corresponding one of the touch switches 92 through 97 (Figure 3) is touched.

The $\overline{A}$ through $\overline{E}$ outputs of the circuit of Figure 7 are applied to the inputs of the circuit of Figure 8. In particular, Figure 8 illustrates decoding logic 222 for generating different outputs in response to the touching of each of the touch sensitive areas 58 through 66 (Figure 3). The decoding logic 222 receives the five lines $\overline{A}$ through $\overline{E}$, and has nine Signal (S) output lines $\overline{S1}$ through $\overline{S9}$. The lines $\overline{S1}$, $\overline{S3}$, $\overline{S5}$, $\overline{S7}$ and $\overline{S9}$ may be considered primary output lines, and the lines $\overline{S2}$, $\overline{S4}$, $\overline{S6}$ and $\overline{S8}$ secondary output lines.

More specifically, the decoding logic 222 is arranged such that when any single touch pad is touched and only one of the input lines $\overline{A}$ through $\overline{E}$ goes low, then an output signal representing the corresponding primary touch sensitive area is generated. Specifically, if the touch pad 85 (Figure 3) is touched, then the $\overline{A}$ line goes low and, at the output of the decoding logic 222, the $\overline{S1}$ primary output line goes low. If the touch pad 86 is touched, the $\overline{B}$ line goes low and at the output of the decoding logic 222, the $\overline{S3}$ primary output line goes low. Similarly, for the touch pad 87, the $\overline{C}$ and $\overline{S5}$ lines go low; for the touch pad 88, the $\overline{D}$ and $\overline{S7}$ lines go low; and for the touch pad 89, the $\overline{E}$ and the $\overline{S9}$ lines go low.

The decoding logic 222 further functions such that when any two adjacent touch pads are simultaneously touched, an output signal representing the secondary touch sensitive area associated with the two pads is produced. For example, if the touch pads 85 and 86 of Figure 3 are simultaneously touched, then the $\overline{A}$ and $\overline{B}$ input lines both go low, and $\overline{S2}$ secondary output line goes low. Other adjacent pairs of the $\overline{A}$ through $\overline{E}$ inputs, when activated, produce corresponding outputs at the $\overline{S4}$, $\overline{S6}$ and $\overline{S8}$ secondary outputs.

The particular decoding logic 222 illustrated and described herein is quite straightforward to implement once the function it performs has been defined. It will therefore be appreciated that numerous variations are possible. Further, the decoding described may be accomplished through a microprocessor control system following suitable instructions stored in a program memory.

Considering now the specific decoding logic 222 of Figure 8, the $\overline{S2}$, $\overline{S4}$, $\overline{S6}$ and $\overline{S8}$ secondary output lines carry the signals representing two adjacent touch pads being touched. To provide these particular outputs, four low activated NAND gates 224 through 227 are provided, each of the low-activated NAND gates 224 through 227 having its two inputs connected to an adjacent pair of the $\overline{A}$ through $\overline{E}$ input lines. The outputs of the low-activated NAND gates 224 through 227 directly supply the secondary output lines $\overline{S2}$, $\overline{S4}$, $\overline{S6}$ and $\overline{S8}$. Each of the low-activated NAND gates 224 through 227 may comprise the equivalent of an SN7402 TTL NOR gate followed by an SN7404 inverter.

The remaining logic elements in the decoding logic 222 serve to ensure that when any single one of the touch switches 93 through 97 (Figure 3) is activated by itself and the corresponding line $\overline{A}$ through $\overline{E}$ goes low, only one of the primary S outputs is activated; and to further ensure that when a "bridged" input occurs, none of the primary outputs $\overline{S1}$, $\overline{S3}$, $\overline{S5}$, $\overline{S7}$ and $\overline{S9}$ are activated.

Generally speaking, NAND gates 228 through 231 serve to ensure that a primary output cannot occur when the next lower secondary output is activated, and the low activated NAND gates 232 through 235 ensure that a primary output cannot occur when the next higher secondary output is activated. Each of the low-activated NAND gates 232 through 235 is connected to drive one of the primary signal output lines $\overline{S1}$, $\overline{S3}$, $\overline{S5}$ or $\overline{S7}$, with the $\overline{S9}$ signal output line being driven directly by the output of the NAND gate 231. To complete the connections required for these functions, each of the NAND gates 228 through 231 has its lower input connected back through one of the inverters 236 through 239 to the $\overline{B}$ through $\overline{E}$ inputs, and its upper inputs connected to the next lower secondary signal output line $\overline{S2}$, $\overline{S4}$, $\overline{S6}$ or $\overline{S8}$. Similarly, each of the low activated NAND gates 232 through 235 has its upper input connected to the output of the corresponding NAND gate 228 through 231 (with the exception of the uppermost low activated NAND gate 232 which has its

input connected directly to the A input line), and its lower input connected back through inverters 240 through 243 to the next higher secondary output lines $\overline{S2}$, $\overline{S4}$, $\overline{S6}$ and $\overline{S8}$.

Since the decoding logic 222 repeats vertically, it is believed that its operation will be completely understood from a description of the operation during several exemplary input conditions, without considering every possible valid input condition. First, the input condition occurring when the primary touch sensitive area 62 (Figure 3) is touched, contacting the touch pad 87 and activating the touch switch 95, will be considered. In Figure 8, only the $\overline{C}$ input line is low and the remaining input lines are high. Since the $\overline{B}$ and $\overline{D}$ input lines are high, the low-activated NAND gates 225 and 226 are not activated, and their outputs remain high. Thus the $\overline{S4}$ and $\overline{S6}$ secondary outputs remain high. The output of the low-activated NAND gate 225 also enables the NAND gate 229 and the output of the low activated NAND gate 226 enables the low activated NAND gate 234 through the inverter 242. With these two last-mentioned NAND gates enabled, the logic low at the input of the inverter 237 is changed to a logic high to activate the NAND gate 229, and the low output thereof activates the low-activated NAND gate 234, producing a logic low output on the $\overline{S5}$ primary output line. All of the other signal output lines remain high.

As another example, if the secondary touch sensitive area 61 (Figure 3) is touched, then the touch pads 86 and 87 are both contacted, activating the touch switches 94 and 95. In this case, the Figure 8 input lines $\overline{B}$ and $\overline{C}$ go low, with the $\overline{A}$, $\overline{D}$, and $\overline{E}$ lines remaining high. Under this condition, the output of the low-activated NAND gate 225 goes low, immediately producing the desired logic low signal output on the secondary signal output line $\overline{S4}$. Even though the $\overline{B}$ input line is also low, no $\overline{S3}$ output is generated because the logic low at the input of the inverter 241 causes a logic high at the output thereof, and the low-activated NAND gate 233 cannot be enabled.

With particular reference now to Figures 9 through 11, the circuitry which receives the Signal ($\overline{S}$) outputs from the decoding logic 222 of Figure 8 will be described.

In Figures 9 and 10, the circuitry receives the $\overline{S}$ lines from the decoding logic 222 of Figure 8, and outputs suitable Lamp (L) signals along the lines L1 through L9 to lamp drivers in Figure 11. Additionally, signals available on the "L" lines are connected to other circuitry (not shown) within the appliance for controlling the actual operation thereof, for example to establish a particular heat setting.

The circuitry of Figure 10 comprises nine individual circuit blocks, each circuit block being built around an operational amplifier connected as a voltage comparator, the nine amplifiers being designated A1 through A9. Each of the "A" amplifiers may comprise an integrated circuit operational amplifier such as a National Semiconductor type number LM301A. The lines $\overline{S1}$ through $\overline{S9}$ are connected through input resistors $R244_1$ through $R244_9$ to the inverting (−) inputs of the respective amplifiers A1 through A9. To prevent input overload at the inverting (−) inputs, each of the input resistors R244 is associated with a lower resistor R246, forming a voltage divider therewith.

To establish a comparison voltage in each of the individual blocks, each includes a reference voltage divider comprising a resistor R248 and a resistor R250 connected between a +5 volt DC source and a circuit ground. The resulting reference voltage is supplied to the non-inverting (+) input of each amplifier "A." Within each of the nine individual circuit blocks (with slight exceptions in the cases of A1 and A9), there are three additional contributions to the magnitude of the reference voltage. The first additional contribution is current flowing from the output terminal through the resistor R252 of each of the amplifiers to the reference voltage point at the non-inverting (+) amplifier input. The resistors R252 are positive feedback resistors and introduce hysteresis to cause each of the nine individual circuit blocks to function as a latch. The second additional contribution to the reference voltage is current flowing from a diode matrix 254 of Figure 9 along unlatch ($\overline{U}$) lines to the reference voltage point. The third additional contribution is current flowing through latch up diodes CR256 and resistors R258 associated with succeeding circuit blocks. The amplifier A9 has no latch-up diode connected to its non-inverting (+) input since there is no succeeding circuit block. Lastly, each of the individual circuit blocks blocks includes a stabilizing resistor R260 connected between the operational amplifier output and circuit ground.

In Figure 9, the diode matrix 254 comprises nine diode groups $G262_0$ through $G262_8$. The cathodes of all the diodes in each group are connected together and to one of the first nine $\overline{S}$ lines from the decoding logic 222 of Figure 8. Each succeeding diode group G262 includes one less diode than the preceding group. The diode anodes are connected to the $\overline{U}$ lines in the following manner: Each of the nine diodes in diode group $G262_0$ is connected to one of the $\overline{U}$ lines. Each of the eight diode anodes in the diode group $G262_1$ is connected to one of the $\overline{U}$ lines $\overline{U2}$ through $\overline{U9}$, omitting $\overline{U1}$. The sequence continues until the last diode group $G268_8$ includes only a single diode with its anode connected to the line $\overline{U9}$, omitting $\overline{U1}$ through $\overline{U8}$.

The operation of Figures 9 and 10 will be better understood if the general functions it must perform are peliminarily mentioned. First, each of the individual circuit blocks of Figure 10 must accept a logic low Signal ($\overline{S}$) input indicating that one of the touch areas 58 through 66 (Figure 3) has been touched and, since a touch is only momentary, must "remember" through a latching action. Second, each of the nine circuit blocks must output a signal along an appropriate Lamp (L) line, both to a lamp driver (Figure 11), and to other circuitry (not shown) within the appliance. Thirdly, the circuitry must cause all the display segments in the array 44 (Figure 3) to the left of the display segment associated with the touch sensitive area which is touched to be energized, doing this by latching up all the lower circuit blocks in the chain. Fourthly, the circuitry must de-energize the display segments by unlatching the circuit Blocks to the right or higher in the chain from the touch sensitive area which is touched.

Now considering the operation specifically, when one of the touch sensitive areas 58 through 66 is touched, the corresponding $\overline{S}$ line goes low, pulling the inverting (−) input of the associated amplifier down below the reference potential supplied to the non-inverting (+) input. This causes the amplifier output to go high and, since the output of each amplifier is connected through a positive feedback resistor R252 back to the non-inverting (+) input, the potential on a non-inverting (+) input is raised sufficiently high to hold the amplifier in a latched on condition, even when the $\overline{S}$ line again goes high.

The output to the display drivers of Figure 11 and to the additional circuitry (not shown) in the appliance is simply taken from the L lines connected to the output of the individual operational amplifiers "A."

In order to latch up lower circuit blocks in the chain when an intermediate touch area, for example the "MED" touch area 62 is touched, a positive voltage flows from the output of the amplifier associated with the touch area which is touched back through the resistor R258 and the diode CR256 to the non-inverting (+) input of the preceding amplifier A, biasing the amplifier sufficiently to cause its output to go high. This sends a signal along the associated L line and, additionally, continues the chain backwards to latch up the next preceding amplifier block, continuing until Amplifier A1 is reached.

Lastly, in order to unlatch succeeding circuit blocks in a chain, the diode matrix 254 of Figure 9 receives the $\overline{S}$ inputs directly from the decoding logic 222 of Figure 8, and additionally receives the "$\overline{OFF}$" line from Figure 7. The diode matrix 254 supplies logic low signals along the $\overline{U}$ lines directly to the non-inverting (+) inputs of the appropriate amplifiers A. These logic low signals are sufficient to overcome the positive voltage supplied to the positive feedback resistors R252, and therefore cause the succeeding amplifier circuits to unlatch.

Referring lastly to Figure 11, there is shown typical circuitry for driving each of the nine display lamps in the array 44 (Figure 3). Since the display drivers are all identical, only the first and ninth are shown, these being designated 262 and 264. The two lamps 266 and 268 are the lamps associated with the display segment 46 and 54 respectively, of Figure 3. In Figure 11, a transformer 270 with its primary winding 272 connected to a suitable source of AC voltage supplies 120 volts AC across its output terminals 274 and 276. Each of the lamps in driver circuits 262 and 264 is connected between the terminals 274 and 276 and is thereby supplied with an AC voltage.

The exemplary circuit 262 comprises a current limiting resistor 278 and a serially controlled rectifier (SCR) 280 connected in series with the neon lamp 266. An input network comprising resistors 282 and 284 is connected to the gate terminal 286 of the SCR 280, the free end of the resistor 288 being connected to the input line L_1. Corresponding elements of the circuit 264 are designated by primed reference numerals.

In the operation of the exemplary circuit 262 of Figure 11, when a positive voltage is supplied to the input terminal L1, the SCR280 is triggered into conduction, causing the neon lamp 266 to light. When the positive input voltage is removed, the SCR 280 ceases conducting, and the lamp 176 is extinguished.

While the specific circuitry described above is intended to operate the embodiment of Figures 1-4, it will be apparent that suitable circuitry to operate the embodiments of Figures 5 and 6 may readily be designed by those skilled in the art of digital logic circuit design, or microprocessor control system design. Accordingly, it is not believed necessary to describe such circuitry in detail herein.

The following table lists component values found suitable for the circuitry of Figures 9 through 11. It will of course be appreciated that these values are exemplary only and are included for the purpose of enabling one skilled in the art to practice the invention.

Semiconductor Devices

A1 - A9	National LM301A integrated circuit operational amplifier
CR256, G262	1N4148
280 & 280'	General Electric C106B SCR

Resistors

278 & 278'	22 K ohms
282 & 282'	330 ohms
284 & 284'	1 K ohms
R244	1 Meg ohms
R246	680 K ohms
R248	1 Meg ohms
R250	1 Meg ohms
R252	820 K ohms
R258	470 K ohms
R260	10 K ohms

From the foregoing it will be apparent that the present invention provides an effective means for alleviating limitations imposed by the minimum panel area required for proper operation of a capacitive touch switch. In particular more individual data entry touch sensitive areas may be provided within a given panel area than would be the case if prior art, unexpanded, capacitive touch switches were employed. As one specific example, the present invention was applied as an improvement to a touch control bar graph.

CLAIMS

1. A touch switch arrangement which permits a high density configuration, said arrangement comprising:

a pair of capacitive touch switches, each of said touch switches having, as the input element thereof, a touch pad of sufficient area for proper operation of the touch switch;

a pair of primary touch sensitive areas arranged such that touch on either primary touch sensitive area activates only one of said touch switches;

a secondary touch sensitive area arranged such that a touch on said secondary touch sensitive area activates both of said touch switches; and

circuit means responsive to said touch switches and including decoding logic for generating different outputs in response to the touching of each of said touch sensitive areas.

2. A touch switch arrangement according to Claim 1, wherein each of said primary touch sensitive areas is positioned over and is smaller than a corresponding one of said touch pads, and wherein said secondary touch sensitive area is positioned at an interface between said touch pads and overlaps both of said touch pads.

3. A touch switch arrangement according to Claim 1, wherein said decoding logic is arranged such that when either touch pad is touched alone an output signal representing the corresponding primary touch sensitive area is generated, and when both of said touch pads are touched at the same time an output signal representing said secondary touch sensitive area is generated.

4. A touch switch arrangement according to Claim 1, wherein said touch pads are adjacent.

5. A touch switch arrangement according to claim 1, wherein said primary touch sensitive areas are spaced from each other and said secondary touch sensitive area is positioned in the space between said primary touch sensitive areas.

6. A linear touch switch array arrangement as claimed in claim 1 comprising a plurality of capacitive touch switches, the touch pads being arranged in the form of a linear array, and the primary and secondary

touch sensitive areas constituting a linear array of touch sensitive areas, whereby fewer touch pads than touch sensitive areas are required and individual touch sensitive areas may have less than the minimum area required for proper operation of a capacitive touch switch.

7. A linear touch switch array arrangement according to claim 6, wherein said primary touch sensitive areas are spaced from each other.

8. A linear touch switch array arrangement according to claim 7, wherein each of said primary touch sensitive areas is positioned over and narrower than its corresponding touch pad.

9. A linear touch switch array arrangement according to claim 8, wherein said secondary touch sensitive areas are positioned in the spaces between said primary touch sensitive areas and overlappingly associated with both of the touch pads corresponding with the adjacent primary touch sensitive areas.

10. A linear touch switch array arrangement according to claim 9, wherein said decoding logic is arranged such that when any single touch pad is touched an output signal representing the corresponding primary touch sensitive area is generated, and when any two adjacent touch pads are simultaneously touched an output signal representing the secondary touch sensitive area associated with the two touch pads is generated.

11. A linear touch switch array arrangement according to claim 6, wheren said decoding logic is arranged such that when any single touch pad is touched an output signal representing the corresponding primary touch sensitive area is generated, and when any two adjacent touch pads are simultaneously touched an output signal representing the secondary touch sensitive area associated with the two touch pads is generated.

12. A touch switch arrangement as claimed in claim 1 further including: a linear array of display segments arranged such that each segment is adjacent to no more than two other segments, said display segments being adapted to be progressively energized to form a bar graph type display to represent a numerical quantity, a linear array of light-transmitting touch sensitive areas superimposed over said linear array of display segments, the circuit means responsive to said touch sensitive areas including means for energizing said display segments such that when any one of said touch sensitive areas is touched a corresponding display segment and all display segments to one side are energized and the remaining display segments are de-energized, wherein the secondary touch sensitive areas are located between a pair of primary touch sensitive areas, each of said primary touch sensitive areas correspondingly to a touch pad forming the input element of a capacitive touch switch, each of said secondary touch sensitive areas are arranged such that a touch thereon activates both of the touch switches corresponding to the adjacent primary touch sensitive areas, and said means for energizing said display segments is responsive to the different output signals of the decoding logic.

13. A touch switch and display arrangement according to claim 12, wherein said decoding logic is arranged such that when any single touch switch is activated an output signal representing the corresponding primary touch sensitive area is generated, and when any two adjacent touch switches are simultaneously activated an output signal representing the secondary touch sensitive area associated with the two touch pads is generated.

14. A switching arrangement comprising:

first and second switch means;

primary and secondary touch areas associated with said switch means, said primary area when touched operative to actuate one of said switch means, and said secondary area operative when touched to actuate both of said switch means; and

decoding means for producing different outputs in response to the actuation of said switch means via said primary and secondary touch areas.

15. A switching arrangement according to claim 14, wherein said switch means comprise capacitive touch switches.

16. A touch switch arrangement as claimed in claim 1 including an arrangement substantially as described herein with reference to any one of the accompanying drawings.

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